IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex Parte PLOFSKY, Jordan

Application for Patent: 10/629,508

Filed: July 29, 2003

Group Art Unit: 2114

Examiner: IQBAL, Nadeem

For:

EMBEDDED MICROPROCESSOR FOR INTEGRATED CIRCUIT TESTING AND DEBUGGING

APPEAL BRIEF

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1. REAL PARTY IN INTEREST

The real party in interest is Altera Corporation, 101 Innovation Drive, San Jose, California 95134.

2. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

3. STATUS OF CLAIMS

The following claims have been rejected and appealed: claims 1-28.

The following claims have been cancelled: None.

The claims on appeal are reproduced below in the Appendix at Section 9 of this Appeal Brief.

4. STATUS OF AMENDMENTS

No amendments were filed subsequent to final rejection.

5. SUMMARY OF CLAIMED SUBJECT MATTER

5.1. Independent Claims 1, 7, 13

All of the independent claims, and the claims dependent therefrom relate to diagnostic testing of a programmable logic device ("PLD").

Independent claim 1 specifically requires "a programmable logic device that comprises a hardcoded microprocessor in communication with programmable logic." In other words, the microprocessor is embedded inside the PLD. Independent claim 7 likewise requires a microprocessor inside the PLD. Independent claim 13 specifically requires "manufacturing a PLD that includes programmable logic, an embedded microprocessor and associated memory."

5.2. Independent Claim 20

Independent claim 20 requires "mounting in a test socket a PLD that includes user logic, an embedded microprocessor and associated memory."

By running testing or debugging routines directly on the PLD using an embedded microprocessor, speed improvements from one thousand times up to one million times may be achieved versus the typical testing utilizing a processor outside of the PLD. Summary, last paragraph.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Ground I:

The rejections presented for review are as follows:

A. The rejections of claims 1-28 under 35 U.S.C. § 102 (e) as being anticipated by U.S. Patent No. 7,020,598 issued to *Jacobson.*

7. ARGUMENT

7.1. Ground I

With respect to Ground I above, the rejected claims are argued as two groups.

7.1.1. Independent Claims 1, 7, 13

***Jacobson* does not teach all of the limitations of each of claims 1-19 and 27-28 ("Group 1").**

Independent claim 1 specifically requires "a programmable logic device comprising... a hardcoded microprocessor in communication with programmable logic." In other words, the microprocessor is embedded inside the PLD. Independent claim 7 likewise requires a microprocessor inside the PLD. Independent claim 13 specifically requires "manufacturing a PLD that includes programmable logic, an embedded microprocessor and associated memory."

Jacobson, however, fails to teach "a PLD that comprises...a hardcoded microprocessor in communication with programmable logic." To the contrary, *Jacobson* teaches away from these claims when it advocates usage of a diagnostic microcontroller (105) *outside* of the PLD (110). *See FIG. 1. See also, e.g., diagnostic microcontroller 105 and PLDs 210, 215, and 220 of FIG. 2 and FIG. 5.*

Jacobson advocates usage of the microcontroller of a "self contained product" or electronic device such as a mobile telephone or PDA, "thereby converting it to a remotely diagnosable/reconfigurable product." *Jacobson Col. 3, lines 60-64.* *Jacobson* further teaches that the electronic device 100 may also be a larger system such as, for example, a satellite. *Col. 3, line 64 to Col. 4, line 4.*

One of skill in the art would understand and recognize a distinction between usage of a microcontroller or processor of a larger electronic device to perform diagnostic tests of a PLD and embedding a special purpose microcontroller into a PLD. Likewise, conversion of an electronic device so that it may use a process of the device to test a PLD is quite different from "manufacturing a PLD that includes programmable logic, an embedded microprocessor and associated memory" (claim 13) so that the PLD can rapidly test itself.

As mentioned in the present application, by running testing or debugging routines directly on the PLD using an embedded microprocessor, speed improvements from one thousand times up to one million times may be achieved versus the typical testing utilizing a processor outside of the PLD. *Summary, last paragraph.*

Note that such an advantage would not be present in the systems taught by *Jacobson*, where the diagnostic processor is *outside* of the PLD.

Further, there can be no confusion between an electronic device and a PLD, as *Jacobson* makes an unmistakable distinction between electronic devices and PLD's that may be included as part of an electronic device. *See e,g, Col. 1, lines 36-54.*

The final Office Action takes the position that the microcontroller being within the same packaging as the programmable logic device anticipates the independent claims that require a microprocessor within a programmable logic device. Applicant disagrees that a microcontroller being next to a programmable logic device is the same thing as a microcontroller being inside the programmable logic device.

The final Office Action at the bottom of page 2 also points out that "The technology today allows multiple processors and programmable logic devices within

the same packaging as is well known in the art." Applicant does not dispute that *Jacobson* shows a diagnostic microcontroller next to a programmable logic device within a larger electronic device such as a mobile telephone. However, even if, *ad arguendo*, the prior art *at the time of the invention*, included electronic devices with multiple processors, such prior art still does not anticipate or teach embedding a processor into a PLD, as uniquely recited by each of independent claims 1, 7, and 13.

Finally, the Final Office Action points out that *Jacobson*, at Col. 15 lines 49-51 discloses "reconfiguring a programmable logic device within the electronic device to act as the diagnostic microcontroller."

Even if an electronic device such as that shown in FIG. 2 of *Jacobson*, comprises multiple PLDs, and one PLD is used as a diagnostic microcontroller, Jacobsen still fails to teach the claim 1 limitation of "a programmable logic device that comprises... a hardcoded microprocessor in communication with programmable logic" and the claim 7 limitation of "a programmable logic device (PLD) comprising ...a hard-coded microprocessor ..." and the claim 13 limitation of "manufacturing a PLD that includes programmable logic, an embedded microprocessor and associated memory."

More specifically, even if programmable logic device 210 of FIG. 2could be reconfigured to function as the diagnostic microcontroller that then would be able to diagnose programmable logic devices 215 and 220, there still would be no microprocessor embedded within one of the programmable logic devices along with programmable logic, memory, a test routine, etc. as required by the varying independent claims.

Since the dependent claims 2-6, 8-12, 14-19, and 27-28 depend from independent claims 1, 7, and 13, it is respectfully submitted that they are each patentable over the art of record for at least the same reasons as set forth above with respect to the independent claims. Further, each of the dependent claims require additional features that when considered in light of the claimed combination further distinguish the claimed invention from the art of record.

7.1.2. Independent Claim 20

***Jacobson* does not teach all of the limitations of each of claims 20-26 ("Group II").**

Independent claim 20 requires "mounting in a test socket a PLD that includes user logic, an embedded microprocessor and associated memory."

As discussed above, *Jacobson* teaches "converting" an electronic device or self contained product into a remotely diagnosable or reconfigurable product. *See. Col. 3, line 60 to Col. 4, line 4.* There are no teachings within *Jacobson* of mounting the PLD within a test socket, and the Examiner has not presented any rationale why this is taught by *Jacobson*. Further, one of skill in the art would not understand the electronic device 100 of *Jacobson* to include a test socket for a PLD, and would not understand *Jacobson* to teach removal of the PLD from the permanent place it occupies in device 100, to any test socket.

Since the dependent claims 21-26 depend from independent claim 20, it is respectfully submitted that they are each patentable over the art of record for at least the same reasons as set forth above with respect to the independent claims. Further, each of the dependent claims require additional features that when considered in light of the claimed combination further distinguish the claimed invention from the art of record.

8. CONCLUSION

In view of the foregoing, all of the claim rejections under 35 U.S.C. § 102 (e) as being anticipated by *Jacobson* cannot stand for at least the reasons discussed. *Jacobson* does not teach all of the limitations of claims of claims 1-19, and 27-28 of Group I and claims 20-26 of Group II.

In view of the foregoing, Appellants respectfully request that the Board reverse the Examiner's rejection of all pending claims. In addition, Appellants believe all claims now pending in this application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

Respectfully submitted,
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9. CLAIMS APPENDIX

CLAIMS ON APPEAL

1. (Original) A programmable logic device (PLD) comprising:

programmable logic that includes test logic;

a port for external communication;

a hard-coded microprocessor in communication with said programmable logic; and

memory that includes a test routine, said memory being in communication with said microprocessor and said programmable logic, whereby said test logic is tested using said test routine under control of said microprocessor.

2. (Original) A PLD as recited in claim 1 wherein said port is a parallel port, a serial port, a USB port or a JTAG port.

3. (Original) A PLD as recited in claim 1 wherein said memory is part of said programmable logic.

4. (Original) A PLD as recited in claim 1 wherein said memory is part of said microprocessor.

5. (Original) A PLD as recited in claim 1 wherein said microprocessor includes an analysis routine for analyzing results of said test routine.

6. (Original) A PLD as recited in claim 1 wherein said microprocessor includes a control routine for controlling execution of said test routine.

7. (Original) A programmable logic device (PLD) comprising:

programmable logic that includes user logic;

a port for external communication;

a hard-coded microprocessor in communication with said programmable logic; and

memory that includes a debugging routine, said memory being in communication with said microprocessor and said programmable logic, whereby said user logic is debugged using said debugging routine under control of said microprocessor.

8. (Original) A PLD as recited in claim 7 wherein said port is a parallel port, a serial port, a USB port or a JTAG port.

9. (Original) A PLD as recited in claim 7 wherein said memory is part of said programmable logic.

10. (Original) A PLD as recited in claim 7 wherein said memory is part of said microprocessor.

11. (Original) A PLD as recited in claim 7 wherein said microprocessor includes an analysis routine for analyzing results of said debugging routine.

12. (Original) A PLD as recited in claim 7 wherein said microprocessor includes a control routine for controlling execution of said debugging routine.

13. (Original) A method of testing a programmable logic device (PLD), said method comprising:

manufacturing a PLD that includes programmable logic, an embedded microprocessor and associated memory;

downloading to said memory a test routine;

executing said test routine under control of said microprocessor to test said programmable logic;

storing raw data resulting from execution of said test routine; and

sending results based on said raw data of said test routine from said microprocessor to a test system external to said PLD, whereby said test system determines the functionality of said PLD.

14. (Original) A method as recited in claim 13 further comprising:

downloading to said microprocessor a control routine for controlling execution of said test routine.

15. (Original) A method as recited in claim 13 wherein said results are said raw data.

16. (Original) A method as recited in claim 13 further comprising:

downloading to said microprocessor an analysis routine for analyzing said raw data from said test routine; and

executing said analysis routine to produce said results, wherein said results reflect conclusions based on said raw data.

17. (Original) A method as recited in claim 13 further comprising:

downloading to said microprocessor a compression routine for compressing said raw data from said test routine;

compressing said raw data; and

sending said compressed raw data as said results.

18. (Original) A method as recited in claim 13 wherein said associated memory is part of said programmable logic.

19. (Original) A method as recited in claim 13 wherein said associated memory is part of said microprocessor.

20. (Original) A method of debugging a programmable logic device (PLD), said method comprising:

mounting in a test socket a PLD that includes user logic, an embedded microprocessor and associated memory;

downloading to said memory a debugging routine;

executing said debugging routine under control of said microprocessor to debug said user logic;

storing raw data resulting from execution of said debugging routine; and

sending results based on said raw data of said debug routine from said microprocessor to a host computer external to said PLD, whereby said host computer determines the functionality of said PLD.

21. (Original) A method as recited in claim 20 further comprising:

downloading to said microprocessor a control routine for controlling execution of said debugging routine.

22. (Original) A method as recited in claim 20 wherein said results are said raw data.

23. (Original) A method as recited in claim 20 further comprising:

downloading to said microprocessor an analysis routine for analyzing said raw data from said debugging routine; and

executing said analysis routine to produce said results, wherein said results reflect conclusions based on said raw data.

24. (Original) A method as recited in claim 20 further comprising:

downloading to said microprocessor a compression routine for compressing said raw data from said debugging routine;

compressing said raw data; and

sending said compressed raw data as said results.

25. (Original) A method as recited in claim 20 wherein said associated memory is part of said user logic.

26. (Original) A method as recited in claim 20 wherein said associated memory is part of said microprocessor.

27. (previously presented) A programmable logic device as recited in claim 1 wherein said hard-coded microprocessor is embedded within said programmable logic device.

28. (previously presented) A programmable logic device as recited in claim 7 wherein said hard-coded microprocessor is embedded within said programmable logic device.

10. EVIDENCE APPENDIX

No evidence has been submitted pursuant to §§ 1.130, 1.131, or 1.132 of 37 CFR, nor has any other evidence been entered by the examiner.

11. RELATED PROCEEDINGS APPENDIX

There have been no decisions rendered by a court or the Board in any proceeding identified pursuant to paragraph (c)(1)(ii) of 37 CFR 41.37(c)(1).